HCMOS family characteristics

FAMILY SPECIFICATIONS

GENERAL

These family specifications cover the common electrical ratings and characteristics of the entire HCMOS 74HC/HCT/HCU family, unless otherwise specified in the individual device data sheet.

INTRODUCTION

The 74HC/HCT/HCU high-speed Si-gate CMOS logic family combines the low power advantages of the HE4000B family with the high speed and drive capability of the low power Schottky TTL (LSTTL).

The family will have the same pin-out as the 74 series and provide the same circuit functions.

In these families are included several HE4000B family circuits which do not have TTL counterparts, and some special circuits.

The basic family of buffered devices, designated as XX74HCXXXXX, will operate at CMOS input logic levels for high noise immunity, negligible typical quiescent supply and input current. It is operated from a power supply of 2 to 6 V.

A subset of the family, designated as XX74HCTXXXXX, with the same features and functions as the “HC-types”, will operate at standard TTL power supply voltage (5 V ± 10%) and logic input levels (0.8 to 2.0 V) for use as pin-to-pin compatible CMOS replacements to reduce power consumption without loss of speed. These types are also suitable for converted switching from TTL to CMOS.

Another subset, the XX74HCUXXXXX, consists of single-stage unbuffered CMOS compatible devices for application in RC or crystal controlled oscillators and other types of feedback circuits which operate in the linear mode.

HANDLING MOS DEVICES

Inputs and outputs are protected against electrostatic effects in a wide variety of device-handling situations. However, to be totally safe, it is desirable to take handling precautions into account
(see also *“HANDLING PRECAUTIONS”*).

RECOMMENDED OPERATING CONDITIONS FOR 74HC/HCT

SYMBOL	PARAMETER	74HC			74HCT			UNIT	CONDITIONS
		min.	typ.	max.	min.	typ.	max.		
V_{CC}	DC supply voltage	2.0	5.0	6.0	4.5	5.0	5.5	V	
V_I	DC input voltage range	0		V_{CC}	0		V_{CC}	V	
V_O	DC output voltage range	0		V_{CC}	0		V_{CC}	V	
T_{amb}	operating ambient temperature range	−40		+85	−40		+85	°C	see DC and AC CHAR. per device
T_{amb}	operating ambient temperature range	−40		+125	−40		+125	°C	
t_r, t_f	input rise and fall times except for Schmitt-trigger inputs		6.0	1000 500 400		6.0	500	ns	V_{CC} = 2.0 V V_{CC} = 4.5 V V_{CC} = 6.0 V

Note

1. For analog switches, e.g. “4016”, “4051 series”, “4351 series”, “4066” and “4067”, the specified maximum operating supply voltage is 10 V.

DC CHARACTERISTICS FOR 74HC

Voltages are referenced to GND (ground = 0 V)

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS		
		74HC										
		+25			−40 to +85		−40 to +125			V_{CC} (V)	V_I	OTHER
		min.	typ.	max.	min.	max.	min.	max.				
V_{IH}	HIGH level input voltage	1.5 3.15 4.2	1.2 2.4 3.2		1.5 3.15 4.2		1.5 3.15 4.2		V	2.0 4.5 6.0		
V_{IL}	LOW level input voltage		0.8 2.1 2.8	0.5 1.35 1.8		0.5 1.35 1.8		0.5 1.35 1.8	V	2.0 4.5 6.0		
V_{OH}	HIGH level output voltage all outputs	1.9 4.4 5.9	2.0 4.5 6.0		1.9 4.4 5.9		1.9 4.4 5.9		V	2.0 4.5 6.0	V_{IH} or V_{IL}	$-I_O$ = 20 μA $-I_O$ = 20 μA $-I_O$ = 20 μA
V_{OH}	HIGH level output voltage standard outputs	3.98 5.48	4.32 5.81		3.84 5.34		3.7 5.2		V	4.5 6.0	V_{IH} or V_{IL}	$-I_O$ = 4.0 mA $-I_O$ = 5.2 mA
V_{OH}	HIGH level output voltage bus driver outputs	3.98 5.48	4.32 5.81		3.84 5.34		3.7 5.2		V	4.5 6.0	V_{IH} or V_{IL}	$-I_O$ = 6.0 mA $-I_O$ = 7.8 mA
V_{OL}	LOW level output voltage all outputs		0 0 0	0.1 0.1 0.1		0.1 0.1 0.1		0.1 0.1 0.1	V	2.0 4.5 6.0	V_{IH} or V_{IL}	I_O = 20 μA I_O = 20 μA I_O = 20 μA
V_{OL}	LOW level output voltage standard outputs		0.15 0.16	0.26 0.26		0.33 0.33		0.4 0.4	V	4.5 6.0	V_{IH} or V_{IL}	I_O = 4.0 mA I_O = 5.2 mA
V_{OL}	LOW level output voltage bus driver outputs		0.15 0.16	0.26 0.26		0.33 0.33		0.4 0.4	V	4.5 6.0	V_{IH} or V_{IL}	I_O = 6.0 mA I_O = 7.8 mA
$\pm I_I$	input leakage current			0.1		1.0		1.0	μA	6.0	V_{CC} or GND	
$\pm I_{OZ}$	3-state OFF-state current			0.5		5.0		10.0	μA	6.0	V_{IH} or V_{IL}	V_O = V_{CC} or GND
I_{CC}	quiescent supply current											
	SSI			2.0		20.0		40.0	μA	6.0	V_{CC} or GND	I_O = 0
	flip-flops			4.0		40.0		80.0		6.0		I_O = 0
	MSI			8.0		80.0		160.0		6.0		I_O = 0
	LSI			50.0		500		1000		6.0		I_O = 0

DEFINITIONS OF SYMBOLS AND TERMS USED IN HCMOS DATA SHEETS

Currents

Positive current is defined as conventional current flow into a device.
Negative current is defined as conventional current flow out of a device.

I_{CC}	Quiescent power supply current; the current flowing into the V_{CC} supply terminal.
ΔI_{CC}	Additional quiescent supply current per input pin at a specified input voltage and V_{CC}.
I_{GND}	Quiescent power supply current; the current flowing into the GND terminal.
I_I	Input leakage current; the current flowing into a device at a specified input voltage and V_{CC}.
I_{IK}	Input diode current; the current flowing into a device at a specified input voltage.
I_O	Output source or sink current: the current flowing into a device at a specified output voltage.
I_{OK}	Output diode current; the current flowing into a device at a specified output voltage.
I_{OZ}	OFF-state output current; the leakage current flowing into the output of a 3-state device in the OFF-state, when the output is connected to V_{CC} or GND.
I_S	Analog switch leakage current; the current flowing into an analog switch at a specified voltage across the switch and V_{CC}.

Voltages

All voltages are referenced to GND (ground), which is typically 0 V**.**

GND	Supply voltage; for a device with a single negative power supply, the most negative power supply, used as the reference level for other voltages; typically ground.
V_{CC}	Supply voltage; the most positive potential on the device.
V_{EE}	Supply voltage; one of two (GND and V_{EE}) negative power supplies.
V_H	Hysteresis voltage; difference between the trigger levels, when applying a positive and a negative-going input signal.
V_{IH}	HIGH level input voltage; the range of input voltages that represents a logic HIGH level in the system.
V_{IL}	LOW level input voltage; the range of input voltages that represents a logic LOW level in the system.
V_{OH}	HIGH level output voltage; the range of voltages at an output terminal with a specified output loading and supply voltage. Device inputs are conditioned to establish a HIGH level at the output.
V_{OL}	LOW level output voltage; the range of voltages at an output terminal with a specified output loading and supply voltage. Device inputs are conditioned to establish a LOW level at the output.
V_{T+}	Trigger threshold voltage; positive-going signal.
V_{T-}	Trigger threshold voltage; negative-going signal.

Analog terms

R_{ON}	ON-resistance; the effective ON-state resistance of an analog switch, at a specified voltage across the switch and output load.
ΔR_{ON}	ΔON-resistance; the difference in ON-resistance between any two switches of an analog device at a specified voltage across the switch and output load.

Capacitances

C_I	Input capacitance; the capacitance measured at a terminal connected to an input of a device.
$C_{I/O}$	Input/Output capacitance; the capacitance measured at a terminal connected to an I/O-pin (e.g. a transceiver).
C_L	Output load capacitance; the capacitance connected to an output terminal including jig and probe capacitance.
C_{PD}	Power dissipation capacitance; the capacitance used to determine the dynamic power dissipation per logic function, when no extra load is provided to the device.
C_S	Switch capacitance; the capacitance of a terminal to a switch of an analog device.

Presettable synchronous 4-bit binary up/down counter

74HC/HCT193

FEATURES

- Synchronous reversible 4-bit binary counting
- Asynchronous parallel load
- Asynchronous reset
- Expandable without external logic
- Output capability: standard
- I_{CC} category: MSI

GENERAL DESCRIPTION

The 74HC/HCT193 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSTTL). They are specified in compliance with JEDEC standard no. 7A.

The 74HC/HCT193 are 4-bit synchronous binary up/down counters. Separate up/down clocks, CP_U and CP_D respectively, simplify operation. The outputs change state synchronously with the LOW-to-HIGH transition of either clock input. If the CP_U clock is pulsed while CP_D is held HIGH, the device will count up. If the CP_D clock is pulsed while CP_U is held HIGH, the device will count down. Only one clock input can be held HIGH at any time, or erroneous operation will result. The device can be cleared at any time by the asynchronous master reset input (MR); it may also be loaded in parallel by activating the asynchronous parallel load input ($\overline{PL}$).

The "193" contains four master-slave JK flip-flops with the necessary steering logic to provide the asynchronous reset, load, and synchronous count up and count down functions.

Each flip-flop contains JK feedback from slave to master, such that a LOW-to-HIGH transition on the CP_D input will decrease the count by one, while a similar transition on the CP_U input will advance the count by one.

One clock should be held HIGH while counting with the other, otherwise the circuit will either count by two's or not at all, depending on the state of the first flip-flop, which cannot toggle as long as either clock input is LOW. Applications requiring reversible operation must make the reversing decision while the activating clock is HIGH to avoid erroneous counts.

The terminal count up ($\overline{TC}_U$) and terminal count down ($\overline{TC}_D$) outputs are normally HIGH. When the circuit has reached the maximum count state of 15, the next HIGH-to-LOW transition of CP_U will cause $\overline{TC}_U$ to go LOW.

$\overline{TC}_U$ will stay LOW until CP_U goes HIGH again, duplicating the count up clock.

Likewise, the $\overline{TC}_D$ output will go LOW when the circuit is in the zero state and the CP_D goes LOW. The terminal count outputs can be used as the clock input signals to the next higher order circuit in a multistage counter, since they duplicate the clock waveforms. Multistage counters will not be fully synchronous, since there is a slight delay time difference added for each stage that is added.

The counter may be preset by the asynchronous parallel load capability of the circuit. Information present on the parallel data inputs (D_0 to D_3) is loaded into the counter and appears on the outputs (Q_0 to Q_3) regardless of the conditions of the clock inputs when the parallel load ($\overline{PL}$) input is LOW. A HIGH level on the master reset (MR) input will disable the parallel load gates, override both clock inputs and set all outputs (Q_0 to Q_3) LOW. If one of the clock inputs is LOW during and after a reset or load operation, the next LOW-to-HIGH transition of that clock will be interpreted as a legitimate signal and will be counted.

PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
3, 2, 6, 7	Q_0 to Q_3	flip-flop outputs
4	CP_D	count down clock input(1)
5	CP_U	count up clock input(1)
8	GND	ground (0 V)
11	$\overline{PL}$	asynchronous parallel load input (active LOW)
12	$\overline{TC}_U$	terminal count up (carry) output (active LOW)
13	$\overline{TC}_D$	terminal count down (borrow) output (active LOW)
14	MR	asynchronous master reset input (active HIGH)
15, 1, 10, 9	D_0 to D_3	data inputs
16	V_{CC}	positive supply voltage

Note

1. LOW-to-HIGH, edge triggered

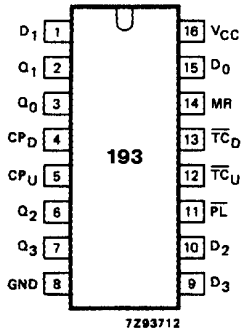


Fig.1 Pin configuration.

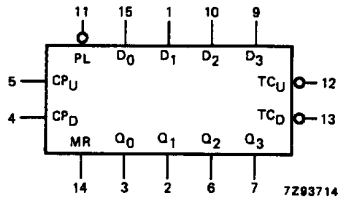


Fig.2 Logic symbol.

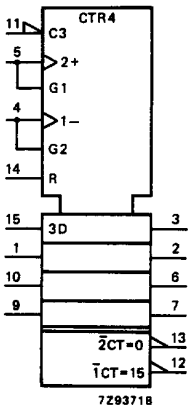


Fig.3 IEC logic symbol.

FUNCTION TABLE

OPERATING MODE	INPUTS								OUTPUTS					
	MR	$\overline{PL}$	CP_U	CP_D	D_0	D_1	D_2	D_3	Q_0	Q_1	Q_2	Q_3	$\overline{TC}_U$	$\overline{TC}_D$
reset (clear)	H H	X X	X X	L H	X X	X X	X X	X X	L L	L L	L L	L L	H H	L H
parallel load	L L L L	L L L L	X X L H	L H X X	L L H H	L L H H	L L H H	L L H H	L L H H	L L H H	L L H H	L L H H	H H L H	L H H H
count up	L	H	↑	H	X	X	X	X	count up				H(2)	H
count down	L	H	H	↑	X	X	X	X	count down				H	H(3)

Notes

1. H = HIGH voltage level
   L = LOW voltage level
   X = don't care
   ↑ = LOW-to-HIGH clock transition
2. $\overline{TC}_U = CP_U$ at terminal count up (HHHH)
3. $\overline{TC}_D = CP_D$ at terminal count down (LLLL)

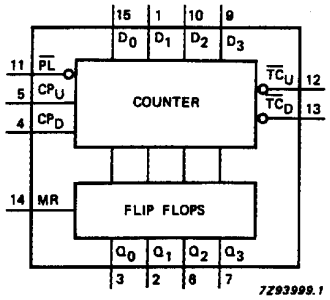


Fig.4 Functional diagram.

(1) Clear overrides load, data and count inputs.

(2) When counting up the count down clock input (CP_D) must be HIGH, when counting down the count up clock input (CP_U) must be HIGH.

Sequence

Clear (reset outputs to zero);

load (preset) to binary thirteen;

count up to fourteen, fifteen, terminal count up, zero, one and two;

count down to one, zero, terminal count down, fifteen,

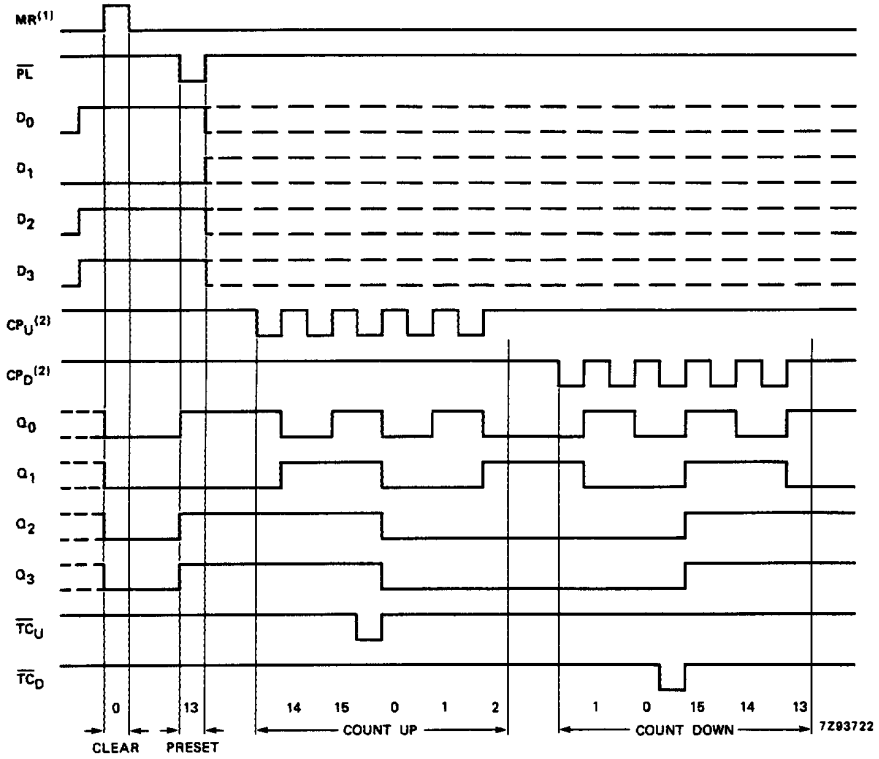


Fig.5 Typical clear, load and count sequence.

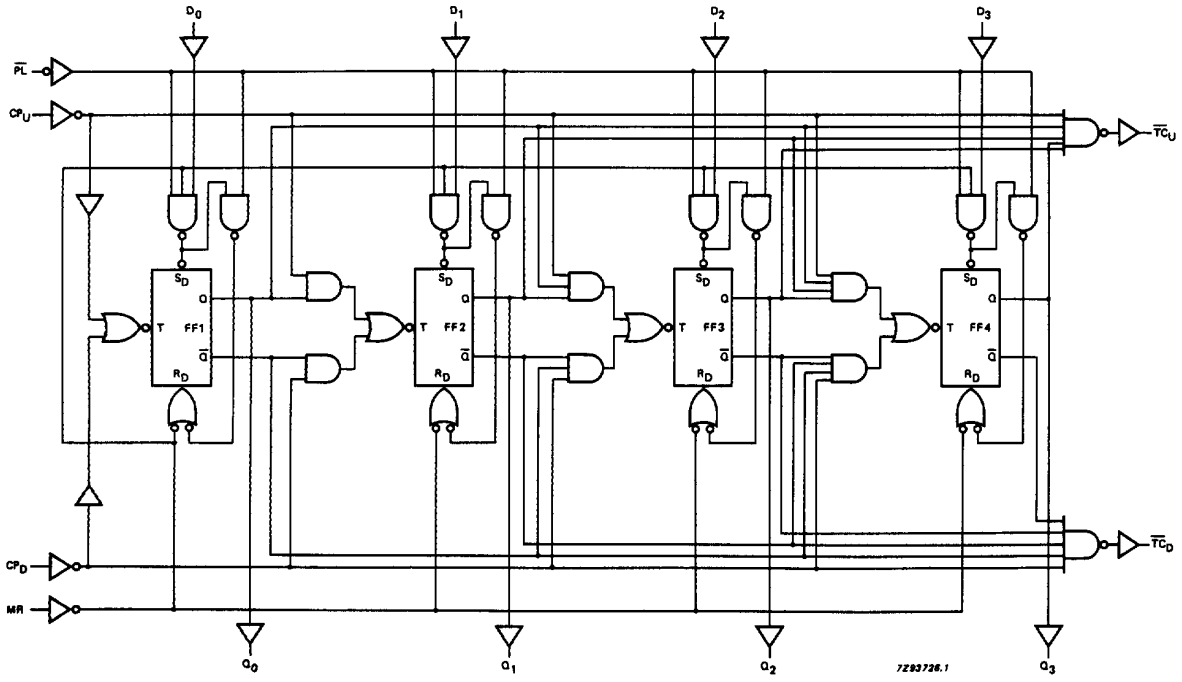


Fig.6 Logic diagram.

DC CHARACTERISTICS FOR 74HC

For the DC characteristics see *"74HC/HCT/HCU/HCMOS Logic Family Specifications"*.

Output capability: standard
I_{CC} category: MSI

AC CHARACTERISTICS FOR 74HC

GND = 0 V; $t_r = t_f$ = 6 ns; C_L = 50 pF

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		74HC								V_{CC} (V)	WAVEFORMS
		+25			−40 to +85		−40 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
t_{PHL}/ t_{PLH}	propagation delay CP_U, CP_D to Q_n		63 23 18	215 43 37		270 54 46		325 65 55	ns	2.0 4.5 6.0	Fig.7
t_{PHL}/ t_{PLH}	propagation delay CP_U to $\overline{TC}_U$		39 14 11	125 25 21		155 31 26		190 38 32	ns	2.0 4.5 6.0	Fig.8
t_{PHL}/ t_{PLH}	propagation delay CP_D to $\overline{TC}_D$		39 14 11	125 25 21		155 31 26		190 38 32	ns	2.0 4.5 6.0	Fig.8
t_{PHL}/ t_{PLH}	propagation delay $\overline{PL}$ to Q_n		69 25 20	220 44 37		275 55 47		330 66 56	ns	2.0 4.5 6.0	Fig.9
t_{PHL}	propagation delay MR to Q_n		58 21 17	200 40 34		250 50 43		300 60 51	ns	2.0 4.5 6.0	Fig.10
t_{PHL}/ t_{PLH}	propagation delay D_n to Q_n		69 25 20	210 42 36		265 53 45		315 63 54	ns	2.0 4.5 6.0	Fig.9
t_{PHL}/ t_{PLH}	propagation delay $\overline{PL}$ to $\overline{TC}_U$, $\overline{PL}$ to $\overline{TC}_D$		80 29 23	290 58 49		365 73 62		435 87 74	ns	2.0 4.5 6.0	Fig.12
t_{PHL}/ t_{PLH}	propagation delay MR to $\overline{TC}_U$, MR to $\overline{TC}_D$		74 27 22	285 57 48		355 71 60		430 86 73	ns	2.0 4.5 6.0	Fig.12
t_{PHL}/ t_{PLH}	propagation delay D_n to $\overline{TC}_U$, D_n to $\overline{TC}_D$		80 29 23	290 58 49		365 73 62		435 87 74	ns	2.0 4.5 6.0	Fig.12
t_{THL}/ t_{TLH}	output transition time		19 7 6	75 15 13		95 19 16		110 22 19	ns	2.0 4.5 6.0	Fig.10
t_W	up, down clock pulse width HIGH or LOW	100 20 17	22 8 6		125 25 21		150 30 26		ns	2.0 4.5 6.0	Fig.7

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		74HC								V_{CC} (V)	WAVEFORMS
		+25			−40 to +85		−40 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
t_W	master reset pulse width HIGH	100 20 17	25 9 7		125 25 21		150 30 26		ns	2.0 4.5 6.0	Fig.10
t_W	parallel load pulse width LOW	100 20 17	19 7 6		125 25 21		150 30 26		ns	2.0 4.5 6.0	Fig.9
t_{rem}	removal time $\overline{PL}$ to CP_U, CP_D	50 10 9	8 3 2		65 13 11		75 15 13		ns	2.0 4.5 6.0	Fig.9
t_{rem}	removal time MR to CP_U, CP_D	50 10 9	0 0 0		65 13 11		75 15 13		ns	2.0 4.5 6.0	Fig.10
t_{su}	set-up time D_n to $\overline{PL}$	80 16 14	22 8 6		100 20 17		120 24 20		ns	2.0 4.5 6.0	Fig.11 note: $CP_U = CP_D$ = HIGH
t_h	hold time D_n to $\overline{PL}$	0 0 0	−14 −5 −4		0 0 0		0 0 0		ns	2.0 4.5 6.0	Fig.11
t_h	hold time CP_U to CP_D, CP_D to CP_U	80 16 8	22 8 6		100 20 17		120 24 20		ns	2.0 4.5 6.0	Fig.13
f_{max}	maximum up, down clock pulse frequency	4.0 20 24	13.5 41 49		3.2 16 19		2.6 13 15		MHz	2.0 4.5 6.0	Fig.7

HT6116-70
CMOS 2K×8-Bit SRAM

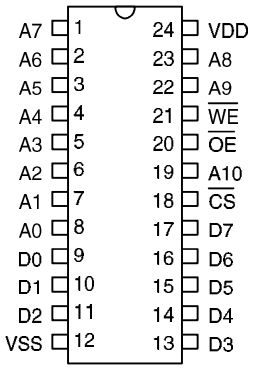
Features

- Single 5V power supply
- Low power consumption
  - Operating: 400mW (Typ.)
  - Standby: 5μW (Typ.)
- 70ns (Max.) high speed access time
- Power down by pin $\overline{CS}$
- TTL compatible interface levels
- Fully static operation
- Memory expansion by pin $\overline{OE}$
- Common I/O using tri-state outputs
- Pin-compatible with standard 2K×8 bits of EPROM/MASK ROM
- 24-pin DIP/SDIP/SOP package

General Description

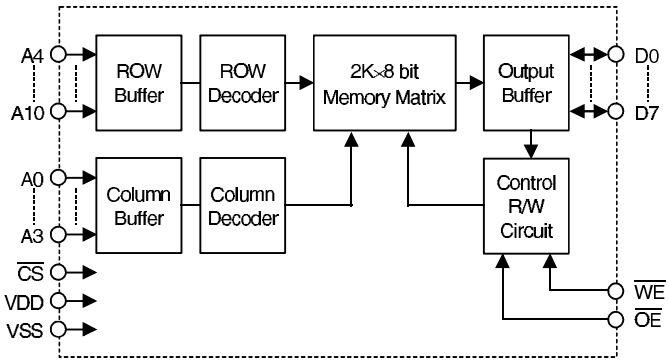
The HT6116-70 is a 16384-bit static random access memory. It is organized with 2048 words of 8 bits in length, and operates with a single 5V power supply. The IC is built with a high performance CMOS 0.8μm process in order to obtain a low standby current and high reliability. The IC contains six-transistor full CMOS memory cells and TTL compatible inputs and outputs, which are easily interface with common system bus structures. The Data bus of the HT6116-70 is designed as a tri-state type. The IC is in the standby mode if the $\overline{CS}$ pin is set to "high".

Pin Assignment



HT6116-70
– 24 DIP/SDIP/SOP

Block Diagram



Pin Description

Pin No.	Pin Name	I/O	Description
8~1, 23, 22, 19	A0~A7 A8, A9, A10	I	Address inputs
9~11 13~17	D0~D2 D3~D7	I/O	Data inputs and outputs
12	VSS	I	Negative power supply, usually connected to the ground
18	$\overline{CS}$	I	Chip select signal pin When this signal is high, the chip is in the standby mode. The chip is in the active mode, if $\overline{CS}$ is low.
20	$\overline{OE}$	I	Output enable signal pin
21	$\overline{WE}$	I	Write enable signal pin
24	VDD	I	Positive power supply

Absolute Maximum Ratings*

Supply Voltage .....–0.3V to +7.0V
Input Voltage..... V_{SS}–0.3V to V_{DD}+0.3V
Storage Temperature.....–50°C to +125°C
Operating Temperature.....–40°C to +85°C

*Note: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only. Functional operation of this device at these or any other conditions above those indicated in the operational sections of this specification is not implied and exposure to absolute maximum rating conditions for extended periods may affect device reliability.

D.C. Characteristics

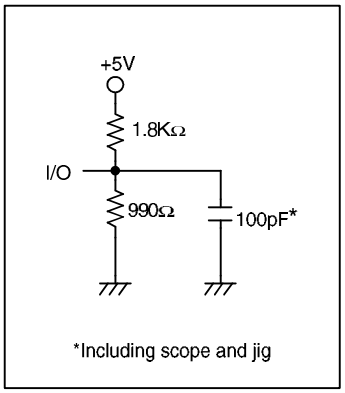
(Ta=25°C)

Symbol	Parameter	Test Conditions		Min.	Typ.	Max.	Unit
		V_{DD}	Conditions				
V_{DD}	Operating Voltage	—	—	4.5	5.0	5.5	V
I_{LI}	Input Leakage Current	5V	V_{IN}=0 to V_{DD}	—	0.1	10	μA
I_{LO}	Output Leakage Current	5V	V_O=0 to V_{DD}	—	0.1	10	μA
I_{DD}	Operating Current	5V	V_{IH}=2.2V, V_{IL}=0.8V In write mode, t_{WC}=1μs.	—	45	90	mA
		5V	V_{IH}=2.2V, V_{IL}=0.8V In read mode, t_{RC}=1μs.	—	80	90	mA
I_{STB}	Standby Current	5V	V_{IH}=2.2V, V_{IL}=0.8V (TTL Input)	—	0.8	1.5	mA
		5V	V_{IH}=4.8V, V_{IL}=0.2V (CMOS Input)	—	0.1	3	μA

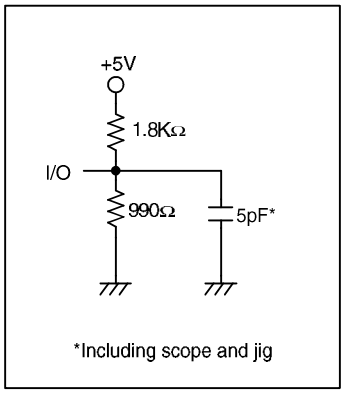
Symbol	Parameter	Test Conditions		Min.	Typ.	Max.	Unit
		V_{DD}	Conditions				
V_{IH}	Input Voltage	5V	—	2.2	2	5.3	V
V_{IL}		5V		–0.3	0.2	0.8	V
I_{OH}	Output Source Current	5V	V_{OH}=4.5V	–1.2	–6.2	—	mA
I_{OL}	Output Sink Current	5V	V_{OL}=0.5V	4.8	14.5	—	mA

A.C. Test Conditions

Item	Condition
Input pulse high level	V_{IH}=3V
Input pulse low level	V_{IL}=0V
Input and output reference level	1.5V
Output load	See Figures below



Output Load



Output Load for
t_{CLZ}, t_{OLZ}, t_{CHZ}, t_{OHZ}, t_{WHZ} and t_{OW}

A.C. Characteristics

Read cycle (V_{DD}=5V±10%, GND=0V, Ta=–40°C to +85°C)

Symbol	Parameter	Min.	Typ.	Max.	Unit
t_{RC}	Read Cycle Time	70	36	—	ns
t_{AA}	Address Access Time	—	35	70	ns
t_{ACS}	Chip Select Access Time	—	35	70	ns
t_{OE}	Output Enable to Output Valid	—	12	40	ns
t_{OH}	Output Hold from Address Change	10	12	—	ns
t_{CLZ}	Chip Enable to Output in Low-Z	10	—	—	ns
t_{OLZ}	Output Enable to Output in Low-Z	10	—	—	ns
t_{OHZ}	Output Disable to Output in High–Z	0	—	30	ns
t_{CHZ}	Chip Disable to Output in High-Z	0	—	30	ns

Note: 1. A read occurs during the overlap of a low $\overline{CS}$ and a high $\overline{WE}$
2. t_{CHZ} and t_{OHZ} are specified by the time when data out is floating

Write cycle (V_{DD}=5V±10%, GND=0V, Ta=–40°C to +85°C)

Symbol	Parameter	Min.	Typ.	Max.	Unit
t_{WC}	Write Cycle Time	70	36	—	ns
t_{DW}	Data Set up Time	20	18	—	ns
t_{DH}	Data Hold Time from Write Time	5	0	—	ns
t_{AW}	Address Valid to End of Write	50	15	—	ns
t_{AS}	Address Setup Time	20	14		ns
t_{WP}	Write Pulse Width	25	0	—	ns
t_{WR}	Write Recovery Time	5	—	—	ns
t_{CW}	Chip Selection to End of Write	35	—	—	ns
t_{OW}	Output Active from End of Write	5	—	—	ns
t_{OHZ}	Output Disable to Output in High-Z	0	—	40	ns
t_{WHZ}	Write to Output in High-Z	0	—	50	ns

Note: 1. A write cycle occurs during the overlap of a low $\overline{CS}$ and a low $\overline{WE}$
2. $\overline{OE}$ may be both high and low in a write cycle
3. t_{AS} is specified from $\overline{CS}$ or $\overline{WE}$, whichever occurs last
4. t_{WP} is an overlap time of a low $\overline{CS}$ and a low $\overline{WE}$
5. t_{WR}, t_{DW} and t_{DH} is specified from $\overline{CS}$ or $\overline{WE}$, whichever occurs first
6. t_{WHZ} is specified by the time when DATA OUT is floating, not defined by output level
7. When I/O pins are data output mode, don't force inverse signals to those pins

Functional Description

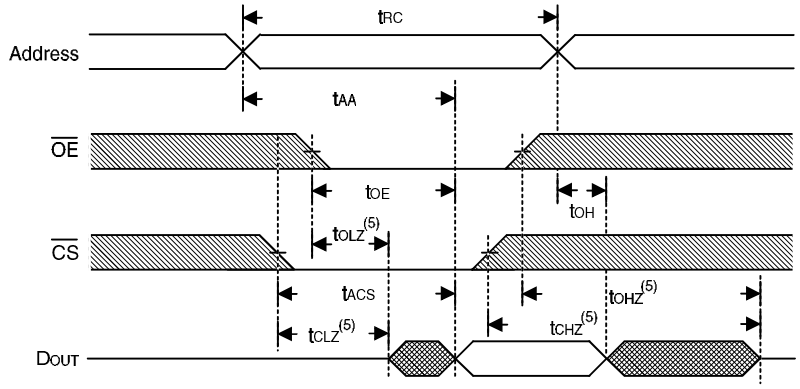
The HT6116-70 is a 2K×8 bit SRAM. When the $\overline{CS}$ pin of the chip is set to "low", data can be written in or read from eight data pins; otherwise, the chip is in the standby mode. During a write cycle, the data pins are defined as the input state by setting the $\overline{WE}$ pin to low. Data should be ready before the rising edge of the $\overline{WE}$ pin according to the timing of the writing cycle. While in the read cycle, the $\overline{WE}$ pin is set to high and the $\overline{OE}$ pin is set to low to define the data pins as the output state. All data pins are defined as a three-state type, controlled by the $\overline{OE}$ pin. In both cycles (namely, write and read cycles), the locations are defined by the address pins A0~A10. The following table illustrates the relations of $\overline{WE}$, $\overline{OE}$, $\overline{CS}$ and their corresponding mode.

$\overline{CS}$	$\overline{OE}$	$\overline{WE}$	Mode	D0~D7
H	X	X	Standby	High–Z
L	L	H	Read	Dout
L	H	H	Read	High–Z
L	X	L	Write	Din

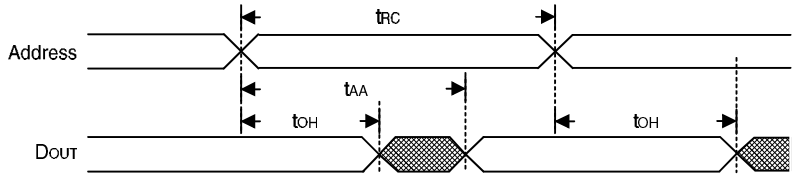
where X stands for "don't care".
H stands for high level
L stands for low level.

Timing Diagrams

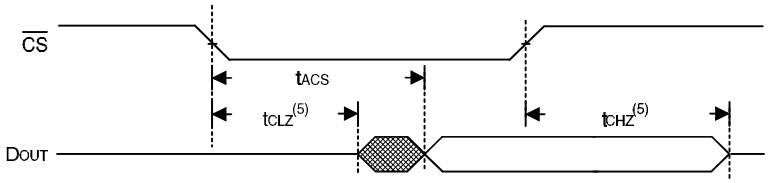
Read cycle (1)



Read cycle (1, 2, 4)



Read cycle (1, 3, 4)



Notes: (1) $\overline{WE}$ is high during the Read cycle

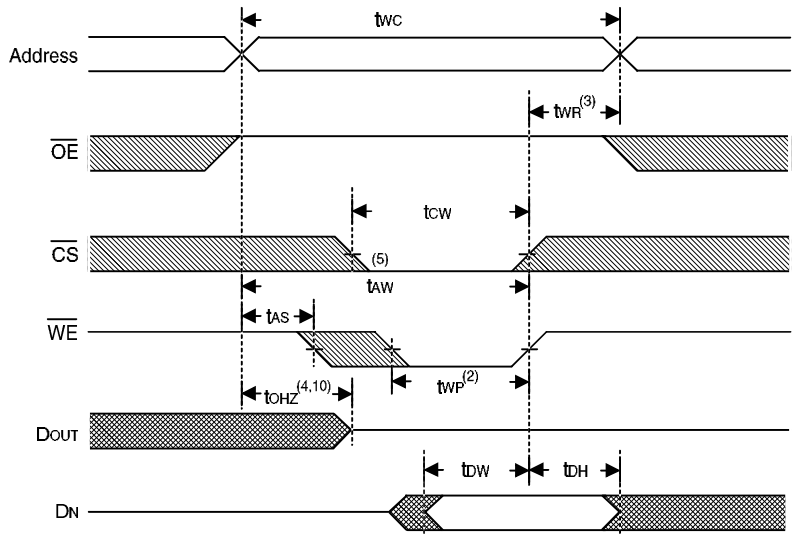
(2) Device is continuously enabled, $\overline{CS}=V_{IL}$

(3) Address is valid prior to or coincident with the $\overline{CS}$ transition low.

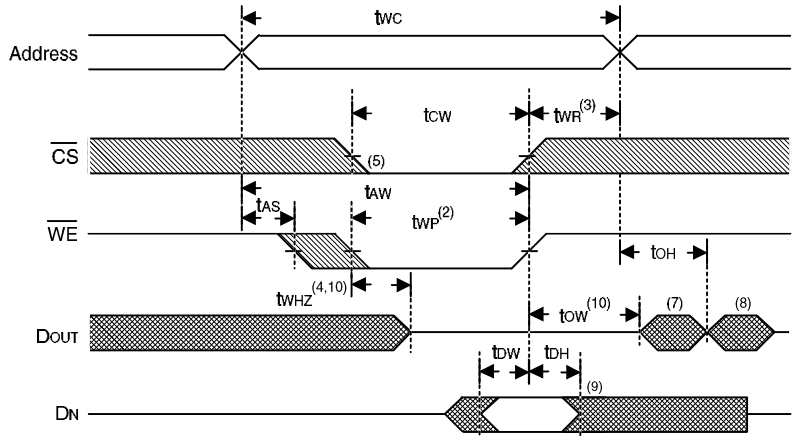
(4) $\overline{OE}=V_{IL}$

(5) Transition is measured±500mV from the steady state.

Write cycle 1 (1)



Write cycle 2 (1, 6)



Notes: (1) $\overline{WE}$ must be high during all address transitions.

(2) A write occurs during the overlap (t_{WP}) of a low $\overline{CS}$ and a low $\overline{WE}$.

(3) t_{WR} is measured from the earlier of $\overline{CS}$ or $\overline{WE}$ going high to the end of the write cycle.

(4) During this period, I/O pins are in the output state, so the input signals of the opposite phase to the outputs must not be applied.

(5) If the $\overline{CS}$ low transition occurs simultaneously with the $\overline{WE}$ low transitions or after the $\overline{WE}$ transition, outputs remain in a high impedance state.

(6) $\overline{OE}$ is continuously low ($\overline{OE}$=V_{IL}).

(7) D_{OUT} is at the same phase of the write data of this write cycle.

(8) D_{OUT} is the read data of the next address.

(9) If $\overline{CS}$ is low during this period, I/O pins are in the output state; then the data input signals of the opposite phase to the outputs must not be applied to them.

(10) Transition is measured ± 500mV from the steady state.

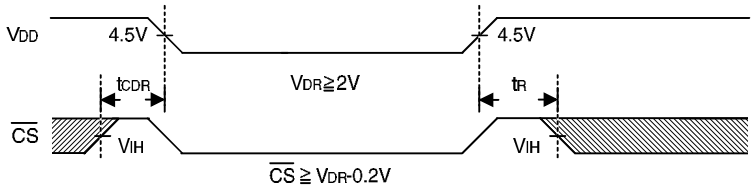
Data Rentention Characteristics

(Ta=–40°C to +85°C)

Symbol	Parameter	Conditions	Min.	Max.	Unit
V_{DR}	V_{DD} for Data Retention	$\overline{CS} \geq V_{DD}$-0.2V	2	5.5	V
I_{CCDR}	Data Retention Current	V_{DD}=3V, $\overline{CS} \geq V_{DD}$-0.2V $V_{IN} \geq V_{DD}$-0.2V or $V_{IN} \leq$ 0.2V	—	50	μA
t_{CDR}	Chip Disable Data Retention Time	See Retention Timing	0	—	ns
t_R	Operation Recovery Time	See Retention Timing	t_{RC}*	—	ns

*t_{RC}=Read Cycle Time

Low V_{DD} Data Retention Timing



GAL16V8

High Performance E²CMOS PLD
Generic Array Logic™

Features

- **HIGH PERFORMANCE E²CMOS® TECHNOLOGY**
  - **— 3.5 ns Maximum Propagation Delay**
  - **— Fmax = 250 MHz**
  - **— 3.0 ns Maximum from Clock Input to Data Output**
  - **— UltraMOS® Advanced CMOS Technology**
- **50% to 75% REDUCTION IN POWER FROM BIPOLAR**
  - **— 75mA Typ Icc on Low Power Device**
  - **— 45mA Typ Icc on Quarter Power Device**
- **ACTIVE PULL-UPS ON ALL PINS**
- **E² CELL TECHNOLOGY**
  - **— Reconfigurable Logic**
  - **— Reprogrammable Cells**
  - **— 100% Tested/100% Yields**
  - **— High Speed Electrical Erasure (<100ms)**
  - **— 20 Year Data Retention**
- **EIGHT OUTPUT LOGIC MACROCELLS**
  - **— Maximum Flexibility for Complex Logic Designs**
  - **— Programmable Output Polarity**
  - **— Also Emulates 20-pin PAL® Devices with Full Function/Fuse Map/Parametric Compatibility**
- **PRELOAD AND POWER-ON RESET OF ALL REGISTERS**
  - **— 100% Functional Testability**
- **APPLICATIONS INCLUDE:**
  - **— DMA Control**
  - **— State Machine Control**
  - **— High Speed Graphics Processing**
  - **— Standard Logic Speed Upgrade**
- **ELECTRONIC SIGNATURE FOR IDENTIFICATION**

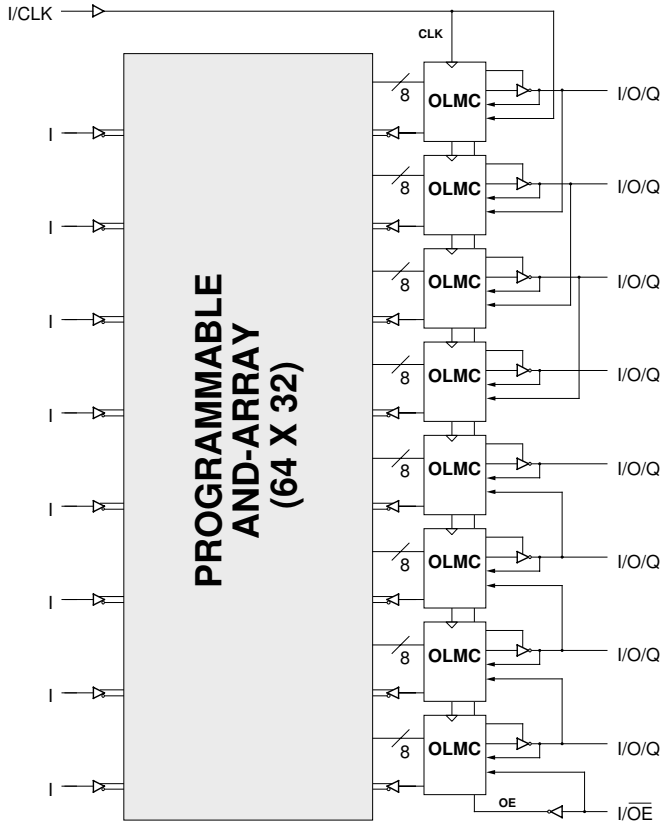
Description

The GAL16V8, at 3.5 ns maximum propagation delay time, combines a high performance CMOS process with Electrically Erasable (E²) floating gate technology to provide the highest speed performance available in the PLD market. High speed erase times (<100ms) allow the devices to be reprogrammed quickly and efficiently.

The generic architecture provides maximum design flexibility by allowing the Output Logic Macrocell (OLMC) to be configured by the user. An important subset of the many architecture configurations possible with the GAL16V8 are the PAL architectures listed in the table of the macrocell description section. GAL16V8 devices are capable of emulating any of these PAL architectures with full function/fuse map/parametric compatibility.

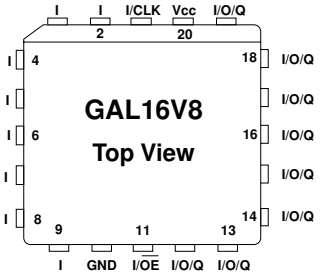
Unique test circuitry and reprogrammable cells allow complete AC, DC, and functional testing during manufacture. As a result, Lattice Semiconductor delivers 100% field programmability and functionality of all GAL products. In addition, 100 erase/write cycles and data retention in excess of 20 years are specified.

Functional Block Diagram

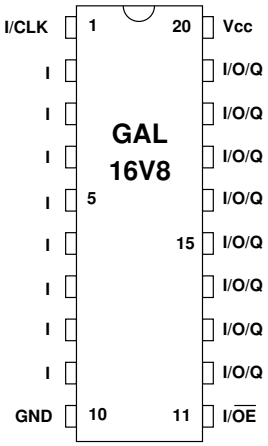


Pin Configuration

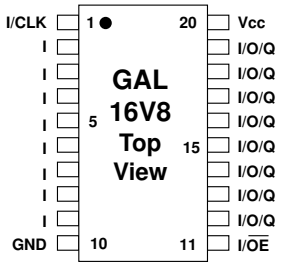
PLCC



DIP



SOIC



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May 2001

Output Logic Macrocell (OLMC)

The following discussion pertains to configuring the output logic macrocell. It should be noted that actual implementation is accomplished by development software/hardware and is completely transparent to the user.

There are three global OLMC configuration modes possible: **simple**, **complex**, and **registered**. Details of each of these modes are illustrated in the following pages. Two global bits, SYN and AC0, control the mode configuration for all macrocells. The XOR bit of each macrocell controls the polarity of the output in any of the three modes, while the AC1 bit of each of the macrocells controls the input/output configuration. These two global and 16 individual architecture bits define all possible configurations in a GAL16V8 . The information given on these architecture bits is only to give a better understanding of the device. Compiler software will transparently set these architecture bits from the pin definitions, so the user should not need to directly manipulate these architecture bits.

The following is a list of the PAL architectures that the GAL16V8 can emulate. It also shows the OLMC mode under which the GAL16V8 emulates the PAL architecture.

PAL Architectures Emulated by GAL16V8	GAL16V8 Global OLMC Mode
16R8	Registered
16R6	Registered
16R4	Registered
16RP8	Registered
16RP6	Registered
16RP4	Registered
16L8	Complex
16H8	Complex
16P8	Complex
10L8	Simple
12L6	Simple
14L4	Simple
16L2	Simple
10H8	Simple
12H6	Simple
14H4	Simple
16H2	Simple
10P8	Simple
12P6	Simple
14P4	Simple
16P2	Simple

Compiler Support for OLMC

Software compilers support the three different global OLMC modes as different device types. These device types are listed in the table below. Most compilers have the ability to automatically select the device type, generally based on the register usage and output enable (OE) usage. Register usage on the device forces the software to choose the registered mode. All combinatorial outputs with OE controlled by the product term will force the software to choose the complex mode. The software will choose the simple mode only when all outputs are dedicated combinatorial without OE control. The different device types listed in the table can be used to override the automatic device selection by the software. For further details, refer to the compiler software manuals.

When using compiler software to configure the device, the user must pay special attention to the following restrictions in each mode. In **registered mode** pin 1 and pin 11 are permanently configured as clock and output enable, respectively. These pins cannot be configured as dedicated inputs in the registered mode.

In **complex mode** pin 1 and pin 11 become dedicated inputs and use the feedback paths of pin 19 and pin 12 respectively. Because of this feedback path usage, pin 19 and pin 12 do not have the feedback option in this mode.

In **simple mode** all feedback paths of the output pins are routed via the adjacent pins. In doing so, the two inner most pins (pins 15 and 16) will not have the feedback option as these pins are always configured as dedicated combinatorial output.

	Registered	Complex	Simple	Auto Mode Select
ABEL	P16V8R	P16V8C	P16V8AS	P16V8
CUPL	G16V8MS	G16V8MA	G16V8AS	G16V8
LOG/iC	GAL16V8_R	GAL16V8_C7	GAL16V8_C8	GAL16V8
OrCAD-PLD	"Registered"[1]	"Complex"[1]	"Simple"[1]	GAL16V8A
PLDesigner	P16V8R[2]	P16V8C[2]	P16V8C[2]	P16V8A
TANGO-PLD	G16V8R	G16V8C	G16V8AS[3]	G16V8

1) Used with **Configuration** keyword.
2) Prior to Version 2.0 support.
3) Supported on Version 1.20 or later.

Registered Mode

In the Registered mode, macrocells are configured as dedicated registered outputs or as I/O functions.

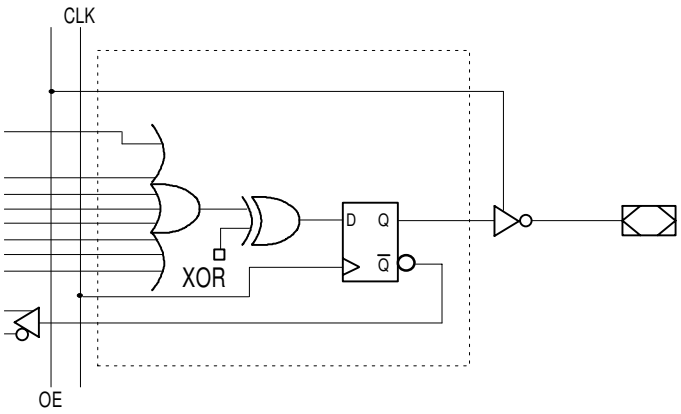
Architecture configurations available in this mode are similar to the common 16R8 and 16RP4 devices with various permutations of polarity, I/O and register placement.

All registered macrocells share common clock and output enable control pins. Any macrocell can be configured as registered or I/O. Up to eight registers or up to eight I/O's are possible in this mode.

Dedicated input or output functions can be implemented as subsets of the I/O function.

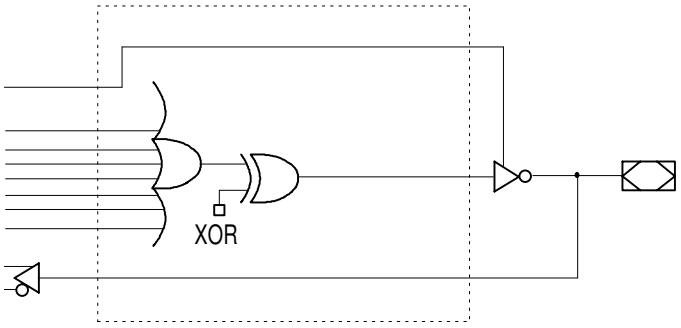
Registered outputs have eight product terms per output. I/O's have seven product terms per output.

The JEDEC fuse numbers, including the User Electronic Signature (UES) fuses and the Product Term Disable (PTD) fuses, are shown on the logic diagram on the following page.



Registered Configuration for Registered Mode

- SYN=0.
- AC0=1.
- XOR=0 defines Active Low Output.
- XOR=1 defines Active High Output.
- AC1=0 defines this output configuration.
- Pin 1 controls common CLK for the registered outputs.
- Pin 11 controls common $\overline{OE}$ for the registered outputs.
- Pin 1 & Pin 11 are permanently configured as CLK & $\overline{OE}$ for registered output configuration.



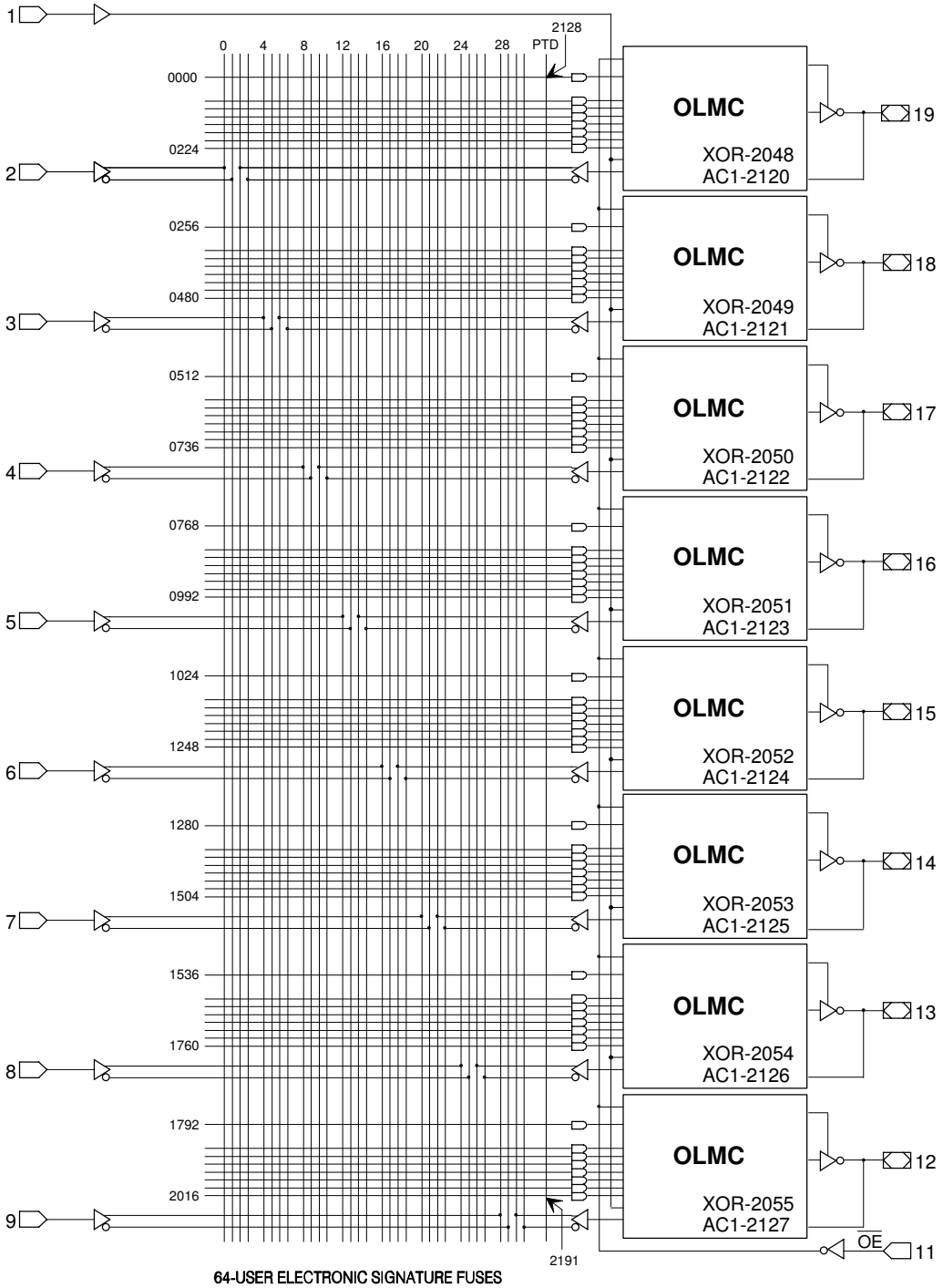
Combinatorial Configuration for Registered Mode

- SYN=0.
- AC0=1.
- XOR=0 defines Active Low Output.
- XOR=1 defines Active High Output.
- AC1=1 defines this output configuration.
- Pin 1 & Pin 11 are permanently configured as CLK & $\overline{OE}$ for registered output configuration.

Note: The development software configures all of the architecture control bits and checks for proper pin usage automatically.

Registered Mode Logic Diagram

DIP & PLCC Package Pinouts



64-USER ELECTRONIC SIGNATURE FUSES

2056, 2057, ...			.... 2118, 2119
Byte 7	Byte 6	.... Byte 1	Byte 0

MSB LSB

SYN-2192
AC0-2193